

**REMARKS/ARGUMENTS**

Claims 5-7, 12, 13, and 17-19 are pending.

Claims 7, 12, and 13, are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5-6, 12 and 17-18 are rejected under 35 U.S.C. §102(b) as being anticipated by Dewey et al. (US Patent 5,724,501), hereinafter Dewey.

Claims 5 and 17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ninomiya et al. (US Publication 2001/0056527 A1), hereinafter Ninomiya in further view of Dewey (US Patent 5,724,501).

Claims 7, 13 and 19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Dewey (US Patent 5,724,501) in further view of La Fetra et al. (US Patent 5,155,828), hereinafter La Fetra.

As to the Section 112 rejection of claim 7, the claim has been amended to recite "acquiring the data from said one of the second cache memories" (line 19). The claim has been amended to recite "in the second control unit" (lines 28 and 29). As amended, the Section 112 rejection of claim 7 is believed to be overcome.

As to the Section 112 rejection of claims 12 and 13, these claims are apparatus claims. The respective preambles as originally filed recited structural limitations of the claimed apparatus, which inadvertently created the basis for the Section 112 rejection. Portions of the preambles have been canceled and incorporated in the main body of the claim. The claims have been amended to cancel "the channel control unit." The claims have been amended to recite "said another channel control unit" to relate to the antecedent recitation of "another channel control unit."

The pending claims have been amended to more clearly recite the disclosed invention. Illustrative embodiments of the pending claims are shown in Figs. 1, 12, and 13, and described in the specification as originally filed beginning on pages 29 and 44. No new matter has been added.

Claim 5 recites in part,

1. a local cache memory disposed in each [of plural] channel control unit[s]
2. a dedicated data transfer path between at least two of the local cache memories
3. writing the data to be written to the local cache memory of a first channel control unit, wherein if the local cache memory does not have sufficient capacity to store the data to be written then first transmitting an amount of data stored in the local cache memory to the global cache memory by way of the connector unit in order to obtain sufficient capacity in the local cache memory to store the data to be written
4. transmitting the data to be written through the dedicated data transfer path to a second channel control unit connected to the first channel control unit [and] writing the transmitted data to the local memory of the second channel control unit

See also pending claims 6, 7, and 17-19, which recite first and second caches, respectively, for local and global caches.

None of the cited references disclose these limitations. Specifically, the references do not disclose local and global caches wherein if the local cache does not have sufficient capacity then some of its data is written to the global cache via a connector unit. The references do not disclose a dedicated data transfer path over which one local cache transmits data to another local cache, which is recited as a *transmitting* step and a *writing* step.

Claim 12 is directed to a channel control unit in a storage control apparatus including a plurality of channel control units, a dedicated path, a connector unit, and a second cache memory, and recites in part for each channel control unit:

1. a first cache memory ..., the first cache memory of at least two of the channel control units being connected to one another by the dedicated data transfer path
2. [a first interface] for transmitting an amount of data from the first cache memory to the second cache memory via the connector unit when the first cache memory has insufficient capacity to store data to be written, the amount of data that is transmitted being sufficient to increase the capacity of the first cache memory

See also claim 13.

None of the cited references disclose a storage control unit having plural channel control units each having a local cache memory, where data in the local cache memory is transmitted to a second cache memory via a connector unit in order to make room in the local

Appl. No. 10/666,709  
Amdt. sent January 18, 2007  
Amendment under 37 CFR 1.116 Expedited Procedure  
Examining Group 2188

PATENT

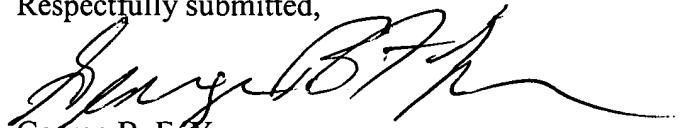
cache memory to store incoming data. None of the cited references disclose a dedicated data transfer path between two of the local cache memories of two channel control units.

**CONCLUSION**

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



George B. F. Yee  
Reg. No. 37,478

TOWNSEND and TOWNSEND and CREW LLP  
Two Embarcadero Center, Eighth Floor  
San Francisco, California 94111-3834  
Tel: 650-326-2400  
Fax: 415-576-0300  
GBFY:jl  
60879961 v1